inseto	**OXIDE COATED WAFER TYPES AND PROPERTIES - SiO_2**	
	ADVANCED TECHNOLOGY FOR RESEARCH & INDUSTRY	**KNOWLEDGE BASE FACT SHEET**

- SCOPE: This article explains the types and primary properties of the most popular semiconductor oxide wafer coating, Silicon Dioxide (SiO_2), and provides example applications.

Silicon Dioxide (SiO_2) coatings provide a dielectric or passivation layer when applied to Silicon (Si), glass and other wafer types used in semiconductors, MEMS, BioMEMS, energy storage devices and other applications.

Correctly specifying the wafer type, its properties and the oxide coating applied, are key to the device being fabricated functioning as intended.

Semiconductor wafers are primarily manufactured from one of the following materials:

- Silicon
- Glass and Fused Quartz
- III-V or II-VI Compound Semiconductors
- Sapphire and Silicon Carbide (SiC)

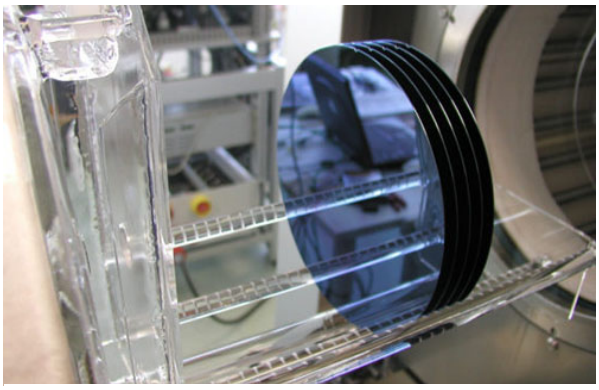
All the above material types can be supplied with coatings of silicon dioxide (SiO_2) or silicon oxynitride (SiO_xN_y) insulators. They can be coated with oxides on one or both sides and coat as well on the polished side, as they do on the etched finish side of a single side polished wafer.

The backside coating can be useful as a masking layer if you are planning to etch through to a layer or to devices fabricated on the front-side; and very good selectivity can be achieved with both wet and dry etch processes.

Wafers of any diameter from 50 to 300mm can be oxide coated with either SiO_2 or SiO_xN_y and can be processed in small or large batch runs, or in single wafer scale reactors, depending on deposition growth rate and quantity of wafers required.

The process and some applications for each insulator material are listed below.

Atmospheric Thermal Oxide – ATOx:



200mm Horizontal oxidation furnace, (image courtesy of ATV)

This coating is one of the oldest semiconductor processes and dates back to the 1950s when Si was first required to be oxidised to produce the insulating layer in MOS devices.

The wafers are typically loaded in lots of 25 into quartz boats, which hold the wafers vertically with a defined space between them. The boats are then processed using tube furnaces where they are slowly heated (to prevent thermal stressing of the Si) to around 1020°C, which is the most commonly used oxidation temperature.

It is then held at this temperature for the time needed to grow the desired thickness of oxide, after which it slowly cools to the idle or room temperature and the boats are unloaded. This method of supporting the wafers during growth dictates that they are almost always oxidised on both sides, and the oxide has to be removed by protecting the front side with resist and striping the backside oxide off using buffered HF (BHF), until the surface becomes hydrophobic again when rinsed.

Si has a great affinity for O_2 and the oxygen readily adsorbs onto the Si surface and is transported across the oxide to the Si interface, where additional SiO_2 grows. Raising or lowering the growth temperature will raise or lower the growth rate significantly. The growth of this family of oxides was modelled by two scientists at Fairchild Semiconductor in 1965, B.E. Deal and A.S. Grove, and is known as the 'Deal-Grove model', used today to predict growth rate.

The oxide grown in this way is Stoichiometric and the refractive index is reliable (1.46 at 632nm). The colours of the films are also very reliable and can easily be viewed under white light and compared against a standard, widely available colour chart.

There are two commonly used thermal oxidation processes; dry oxide and wet oxide.

Dry oxide is used when the desired oxide thickness is small, as the process is slow and the growth rate for <100> Si is typically 80 to 100nm.hr-1 at 1020^{o}C. Raising or lowering the growth temperature will raise or lower the growth rate significantly. As the name suggests, a dry oxide process uses a dry source of molecular oxygen, such as a compressed gas tank. The oxygen tanks will have no water contamination and the resulting oxidation process produces a less porous SiO_2 film.

A wet oxide process runs with steam as the precursor, which is obtained by bubbling the O_2 feed-gas through a heated flask of DI water until it is saturated. The addition of H_2O into the process increases the rate of growth for <100> Si to 290-310nm.hr-1 at 1020^{o}C.

Hydrochloric acid (HCl) can be used for the removal of native oxide from the Si before oxide growth and this reduces the density of states at the oxide/Si interface and improves its performance as a dielectric. The presence of HCl also increases the growth rate of the oxide layer.

The presence of H in the wet process increases the transport rate across the oxide to the interface. The resulting oxide is grown both into the Si as well as on top of it at a ratio of 46% into the surface and 54% on top of the original Si surface. In other words, the overall wafer thickness does not increase by the depth of the oxide layer, as some of the Si is consumed during the oxidation process.

Another factor that influences the growth rate is the Si crystal orientation, with <111> Si having a growth rate of about 1.7x that of <100> Si. This is due to there being more Si atoms available on the <111> plane and hence the reaction with O_2 is faster. Finally, highly doped Si (at about 10E19 to 10E20.cm-3) also oxidises faster than less doped Si.

Thermally grown oxide usually has compressive stress at the surface due to the differences in thermal expansion between Si and SiO_2 and about 300MPa is typical.

Plasma Enhanced Chemical Vapour Deposition, PECVD SiO_2:

This is the other most common oxide wafer growth technique and was developed as a means of growing good quality oxide coated interlayer dielectric material at relatively low temperatures, compatible with metallization schemes.

Precursors of Silane (SiH_4) and N_2O are mixed and then fed into a vacuum chamber and excited using a 13.56MHz RF source. The electrode with the wafers sat on it is held at 350 to 400^{o}C and the oxide forms by a thermally catalysed reaction of the excited gas states to form SiO_2. A liquid precursor, Tetraethyl Orthosilicate $Si(C_2H_5O)_4$ (TEOS), can also be used. This avoids using Silane/Dichlorosilane and can also reduce the levels of stress in the SiO_2 film.

Stress can be controlled by adjusting the SiH_4:O_2 ratio of the feed gases and ranges from 50 to 300MPa compressive, which is comparable to stresses produced by the thermal oxidation processes.

The growth rate is less dependent on orientation and doping level and the film composition can be adjusted to be tensile or compressive. Growth rates are typically in the 300 to 400nm.min-1 range, so it is a faster process than the higher temperature thermal techniques.

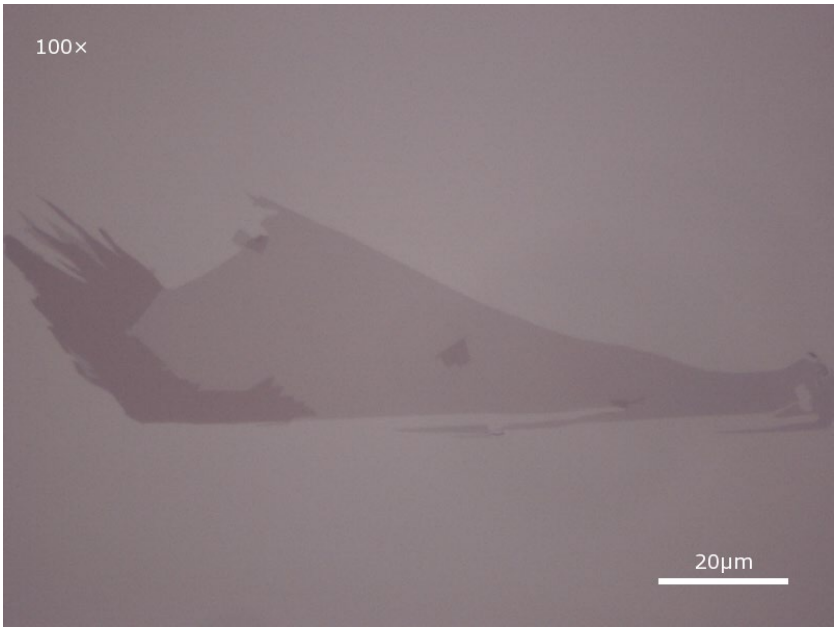
The key advantage of this technique is the lower temperature of growth which, at 350 to 400^{o}C, is compatible with aluminium when used for interlayer dielectric and passivation. The main disadvantage (or advantage, depending on the number of wafers required) is that most of these reactors are cylindrical chambers with flat electrodes, so the number of wafers that can be processed simultaneously is much lower than in a tube furnace.

Applications:

There are numerous applications of thermal oxide ranging from its use as an insulator, an implant or etch mask and an etch stop layer in SOI wafers, as well as part of a passivation layer stack. However, ATOx has some limitations due to the high temperature of growth so, in a passivation layer, the underlying metal layers must be refractory metals to withstand the growth temperature.

The optical properties make thermal oxide very good for photonics devices and also as a coating on Si wafers, which enable very good contrast to flakes of 2D materials that are exfoliated onto them, as well as providing underlying insulation for mobility measurements. An example of this can be seen below, where monolayers and a few layer graphene flakes just a few μm wide can clearly be seen.

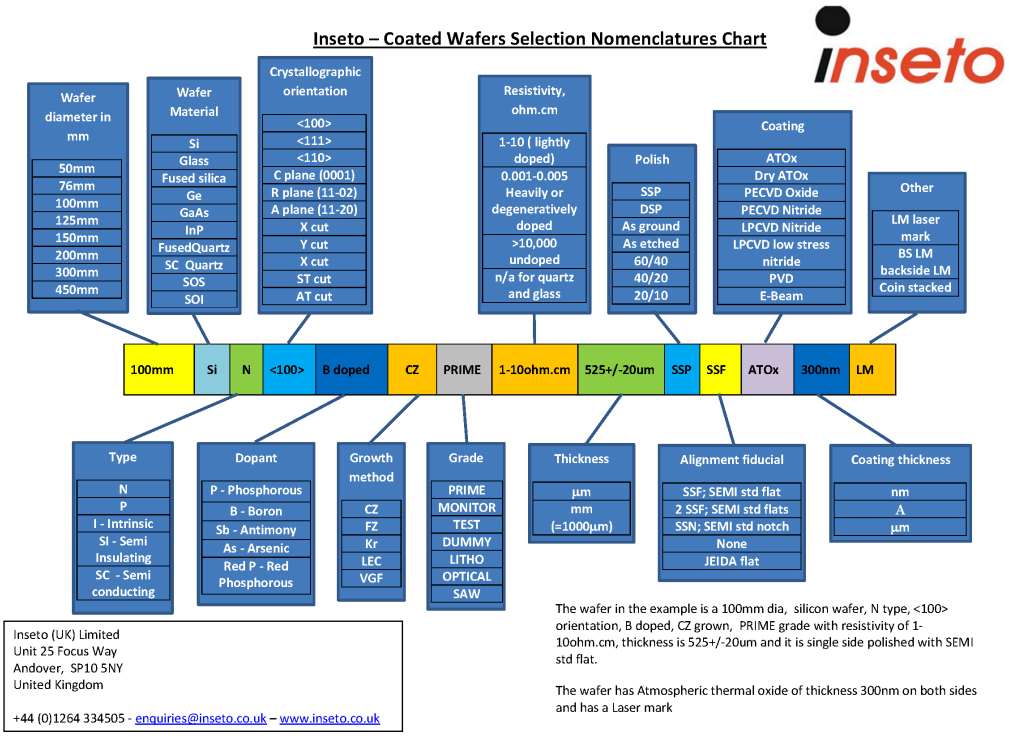
A typical example of PECVD grown oxide is in very high integrity passivation layers, where the ability to add in NH_3 to the process enables SiO_xN_y silicon oxynitride to be produced in a single process step, which produces an excellent passivation layer rather than growing sandwiches of SiO_2 and Si_3N_4.



Single and bi-layer graphene flakes on 90nm of thermally grown SiO_2, (image courtesy of Graphene Industries Ltd)

In need of oxide coated wafers?

Inseto stocks, supplies and produces a wide range of wafer types and with different oxide thicknesses, on a fast delivery service. In addition, we can produce coated wafers with custom thickness oxide layers. The figure below shows our nomenclature chart for coated wafers:



Inseto's oxide-coated wafers inventory can be found in our online store and further information about semiconductor wafers can be found in our Knowledge Base on our website. Further reading on oxide processes etc., can be found in: VLSI Technology, edited by S.M. Sze, the chapter on oxidation and online resources including: Wikipedia and Libretexts.